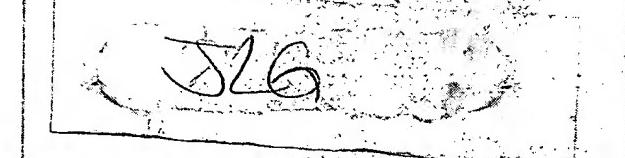


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109-898752
07/03/04

708	626
Class	Subclass
ISSUE CLASSIFICATION	



PATENT NUMBER	
6,065,626	

U.S. UTILITY Patent Application

M.S.

O.I.P.E.

PATENT DATE

SCANNED

K52 OA JUN

APPLICATION NO. 09/898752	CONT/PRIOR F	CLASS 708	SUBCLASS 626	ART UNIT 2121	EXAMINER Malzahn
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APPLICANTS
Sunil Talwar
Dmitriy RumyninTITLE
Multiplication logic circuitPTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)		
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)	
708	626	708	210	
INTERNATIONAL CLASSIFICATION				
G 06 F 7/50				
<input type="checkbox"/> Continued on Issue Slip Inside File Jacket.				

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. 8	Figs. Drwg. 10	Print Fig. 5	Total Claims 5	Print Claim for O.G. 1
<input type="checkbox"/> The term of this patent, subsequent to _____ (date) has been disclaimed. <input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent No. _____ <input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.			NOTICE OF ALLOWANCE MAILED 05/25/04		
			DAVID H. MALZAHN PRIMARY EXAMINER (Primary Examiner) 5/22/04 (Date)		
 (Legal Instruments Examiner)			ISSUE FEE Amount Due \$1665.00 Date Paid		
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